A 44-GHz Monolithic Waveguide Plane-Wave Amplifier with Improved Unit Cell Design

Youngwoo Kwon, *Member, IEEE*, Emilio A. Sovero, *Member, IEEE*, Don S. Deakin, and J. Aiden Higgins, *Senior Member, IEEE*

***Abstract*— A 44-GHz monolithic waveguide plane-wave amplifier (PWA) with improved unit cell design is presented in this paper. The unit cell is a two-stage direct-coupled design and satisfies size, biasability, and stability requirements of the waveguide PWA. The ultra-compact unit cell had a cell size of 0.8 mm^2, and showed a small-signal gain of 8 dB and an output power of 15 dBm at 44 GHz with a corresponding dc-to-RF efficiency of 10%. A monolithic waveguide PWA using these unit cells showed a "flange-to-flange" gain of 5 dB, an output power of 0.3 W, and an efficiency of 2% at 44 GHz.**

***Index Terms*—High electron-mobility transistors, power amplifiers, power combining, quasi-optic techniques.**

I. Introduction

SPATIAL power combining by quasi-optic techniques based on the grid and active-array approach is a promising concept for getting watt-level power at millimeter-wave frequencies. This method has the potential of achieving higher combining efficiencies than conventional methods using transmission lines. An attractive feature of spatial power combining is that the output power scales linearly with the chip size. This means that the output power can be increased by increasing the chip size or by simply tiling chips. Recently, a number of groups have demonstrated monolithic quasi-optic amplifiers at millimeter-wave frequencies. Free-space power combining using the monolithic grid approach was demonstrated up to U-band [1], [2]. Waveguide plane-wave amplifiers (PWA's), where power combining occurs inside the waveguide, were also realized in monolithic-microwave integrated-circuit (MMIC) form at millimeter waves. The waveguide PWA approach is of practical interest since it does not suffer from any diffraction losses. It can also be easily inserted into current millimeter-wave transceiver systems using standard waveguide flanges. Initial results of a waveguide PWA have recently been reported. Waveguide PWA's using heterojunction bipolar transistors (HBT's) have shown a positive gain at 49 GHz [3], and another PWA using pseudomorphic high electron-mobility transistors (pHEMT's) have shown 3-dB gain at 42 GHz [4]. However, they have failed to show more reasonable gain at the design frequency of 44 GHz.

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Quasi-optic power amplifiers consist of passive combining structures such as antenna arrays and active unit cells, which provide power amplification. So far, extensive study has been performed on passive antenna structures. These include dipoles, patches, and slots [5]–[8]. Unlike the passive structures, little has been addressed on the design of active unit cells. Unit cells of most quasi-optic amplifiers have been unmatched single transistors with only bias structures. Also, multiple-stage amplification has rarely been tried at the unit cell level. However, multiple-stage unit cells are often necessary for millimeter-wave applications where the gain of a single device is limited.

This paper reports on 44-GHz waveguide PWA's using improved unit cell design. The proposed unit cell design is a fully matched two-stage design based on a direct-coupled topology. The unit cell showed a small-signal gain of 8 dB and an output power of 15 dBm at 44 GHz. Unit cell size was only 0.8 mm^2. These unit cells were employed together with improved antenna design to demonstrate a waveguide PWA with a "flange-to-flange" gain of 5 dB at the design frequency of 44 GHz.

II. Unit Cell-Design Considerations

Special requirements of the cell design for quasi-optic amplifiers can be summarized as follows:

1) compactness;
2) biasability;
3) stability.

The size of unit cell is an important design parameter for quasi-optic amplifiers. Smaller cell size generally means more unit cells per given area and, therefore, higher output power. This also means more power at reduced chip cost. Moreover, there is a hard limit on the unit cell size for waveguide spatial power-combining methods, which is of prime interest in this paper. The concept of waveguide power combining was shown in [3]. Since the wave impinges on the wafer obliquely inside the waveguide, scan blindness may occur. To prevent surface-wave excitation, the antennas have to be spaced close enough, which means that the unit cells have to be smaller than a certain size. For our case of input slot-antenna and output patch-antenna combinations, allocated unit-cell size was only 0.8 mm^2 (0.64 mm $\times$ 1.25 mm). Multiple-stage design in a limited chip size imposes a great challenge for the designer.

Our goal was to design a two-stage unit cell in a very limited chip area. One of the nontrivial problems is biasing. It is

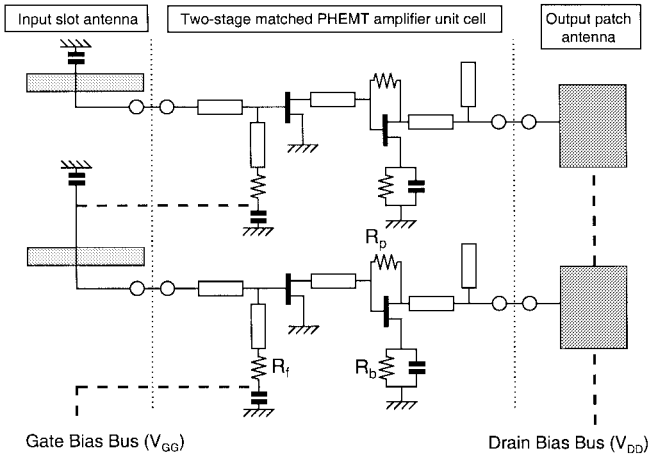

Fig. 1. Equivalent-circuit schematic of unit cell and bias connections between unit cells. Solid lines are RF signal lines and dashed lines are dc bias lines.

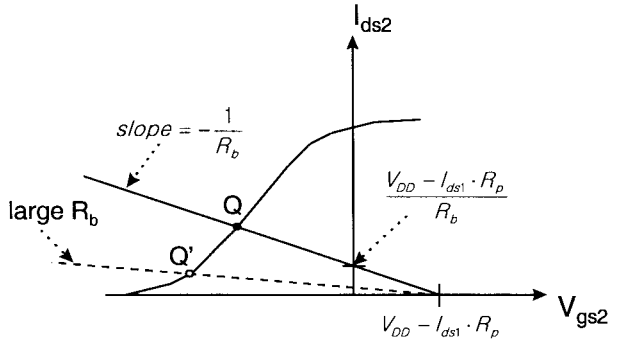

Fig. 2. $I_{\rm ds}$ versus $V_{\rm gs}$ characteristics of the second-stage FET illustrating the bias-point dependence on R_b.

impossible to use individual bias circuits for the gate and drain terminals of each transistor due to size constraint. The bias decoupling circuit based on a conventional $\lambda/4$-transformer with an RF short is also out of question; $\lambda/4$ at 44 GHz for a 50-Ω line on a 75-μm-thick GaAs substrate is about 600 μm, comparable to the dimension of the unit cell. Another design challenge related to biasing is the bias connection between cells; the whole array has to be biased with a single bias bus. Cell-to-cell bias connections should, therefore, be considered during chip layout to prevent dc bias lines from crossing or interfering with signal lines.

Stability is another big concern in quasi-optic amplifiers. Coupling between unit cells and uncertainty in the impedances of the antennas complicate the design. Absolute stability should, therefore, be guaranteed at both in-band and out-of-band frequencies to keep amplifier arrays from unwanted oscillations. Resistive feedback techniques are commonly used for this purpose [1], [7]. However, for millimeter-wave applications, feedback design has to account for subsequent gain degradation; since the device gain is limited at millimeter-wave frequencies, too much feedback may result in an unacceptable amplifier gain. There should be a compromise between stability and gain.

III. Unit Cell Design

In this paper, a direct-coupled feedback topology was employed and optimized to satisfy size, biasing, and stability requirements of the waveguide PWA's. The schematic of the unit cell is shown in Fig. 1. Also shown in Fig. 1 are bias connections to adjacent unit cells. The design goal was to achieve at least 8-dB small-signal gain with 40-mW output power per unit cell. The first step of the design was the choice of active devices. Maximum available gain of our pHEMT's used in this paper was approximately 6 dB at 44 GHz. Two stages were thus needed to achieve 8-dB gain. To estimate the output power per gatewidth, power simulations were performed using a custom nonlinear pHEMT model [9]. Based on the simulation results, 80 and 160 μm were used for the first- and the second-stage field-effect transistor (FET), respectively.

As stated earlier, it was impossible to separately bias the gate and drain of each transistor due to tight size constraint. A direct-coupled topology was used to simplify the bias circuitry, as well as to improve stability. The drain terminal of the first-stage FET and the gate terminal of the second-stage FET were connected without dc blocking capacitors. The drain bias of the first-stage FET was thus applied from the drain bias of the second-stage FET via a parallel feedback resistor (R_p in Fig. 1). This resistor was also a negative-feedback element and served as a means to improve the stability of the second-stage FET. A resistor value of 200 Ω was chosen as a good compromise between stability and gain. The first-stage drain bias was then given by

$$V_{\rm ds1} = V_{\rm DD} - R_p \cdot I_{\rm ds1}. \tag{1}$$

The first-stage drain current ($I_{\rm ds1}$) and drain voltage ($V_{\rm ds1}$) was controlled by the input gate bias (V_{GG}). Decreasing V_{GG} toward pinchoff voltage resulted in smaller $I_{\rm ds1}$ and, thus, higher $V_{\rm ds1}$.

The source bias resistor (R_b in Fig. 1) was employed to self-bias the second-stage HEMT. The second-stage gate bias circuitry was, in this way, eliminated. The value of the second-stage source bias resistor (R_b) was determined from the following coupled equations:

$$I_{\rm ds2} = \frac{1}{R_b}(V_{DD} - I_{\rm ds1} \cdot R_p - V_{\rm gs2}) \tag{2}$$

$$I_{\rm ds2} = \mathcal{F}(V_{\rm gs2}) \tag{3}$$

where $\mathcal{F}(V_{\rm gs2})$ is the drain saturation current versus gate voltage characteristics of the second-stage HEMT. The two equations can be graphically represented in the $I_{\rm ds2}$–$V_{\rm gs2}$ plane, as shown in Fig. 2. The intersection point (Q in Fig. 2) of the two curves is the operating point. By changing R_b, the slope of the line changes and so does the operating point; operating point moves to Q in Fig. 2 as R_b is increased. Larger R_b results in a class-B-like bias and vice versa. It can also be shown from Fig. 2 that unlike $I_{\rm ds1}$, $I_{\rm ds2}$ increases with decreasing V_{GG}.

Stability of the first-stage HEMT was improved by employing lossy matching at the input. A combination of a small resistor ($R_f = 10\ \Omega$ in Fig. 1), bypass capacitor, and section

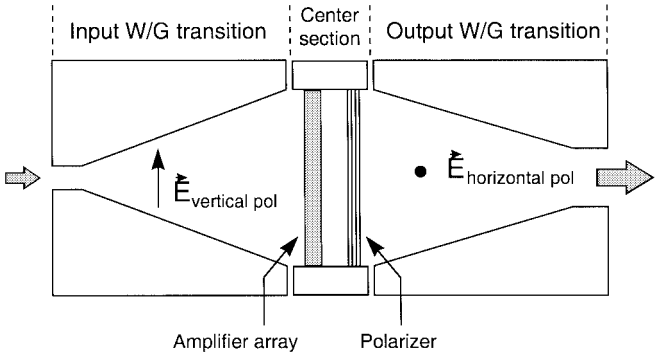

Fig. 3. Schematic diagram showing the concept of the array amplifier in a waveguide.

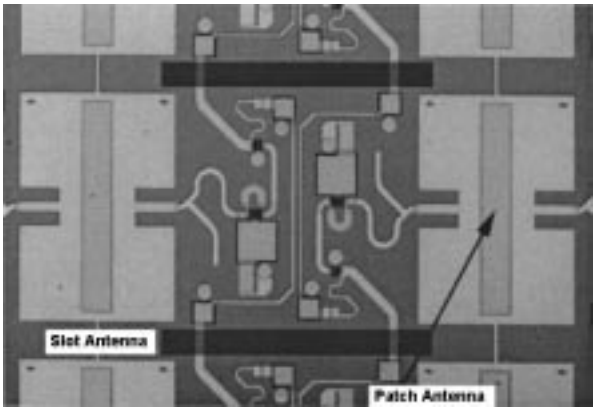

Fig. 4. Photograph of the fabricated chip showing the details of the amplifier cell and antennas. Slot antennas are added to the photograph for a better understanding of the structure.

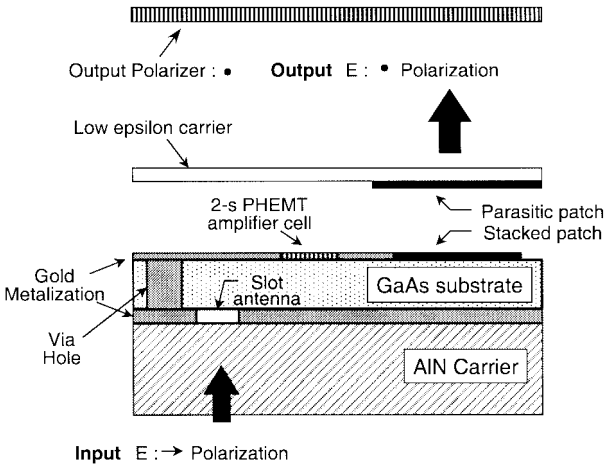

Fig. 5. Cross section of the elementary PWA cell.

of a microstrip line was used for this purpose. This lossy matching structure served to improve low-frequency stability and to equalize the amplifier gain. It also served as a part of the input-matching circuit to the slot antenna whose input impedance was $12-j50\ \Omega$. A section of a microstrip line was inserted between the gate and resistor to minimize the gain degradation effect due to lossy matching at 44 GHz; the length of this transmission line was close to $\lambda/4$ at 44 GHz, and thus transformed the low impedance of the resistor to the high impedance at the gate terminal, resulting in minimum power loss at 44 GHz. Output matching to the patch antenna was realized with a simple single-stub topology using microstrip lines. Lossy matching was avoided at the output to maximize the output power. The input impedance of the patch antenna was close to 50 Ω at 44 GHz.

Also shown in Fig. 1 are bias connections between the unit cells. The drain bias (V_{DD}) was applied through the patch antennas; bias bus lines were connected to the virtual ground point of the patch antenna for bias decoupling. The gate biases were connected to adjacent cells, as indicated in Fig. 1. Line crossing or interference with RF lines was avoided in this way.

IV. Waveguide PWA Design

The structure of waveguide PWA is illustrated in Fig. 3. The PWA consists of a pair of waveguide fixtures and a center section carrying the amplifier chip. The center section is an oversized square waveguide with a size of ~10 mm $\times$ 10 mm, which approximately corresponds to the size of the amplifier chip. The fixture consists of a transition from the standard U-band waveguide (WR-19) to the oversized square waveguide of the center section. Isolation between the input and output ports was achieved by employing different polarizations at each port; the input fixture was vertically polarized while the output fixture was horizontally polarized. A polarizer was placed downstream from the center section; i.e., along the output guide. The polarizer was used to prevent the leakage of the input signal into the output waveguide. It also helped to remove the gain ripple during measurement and provided a small amount of input tuning by adjusting its position.

The MMIC amplifier chip consisted of 56 unit cells arranged in a 7 $\times$ 8 array configuration. A photograph showing the details of the unit cells is shown in Fig. 4. Slot antennas are added in the photograph for a better understanding of the structure. Each unit cell contained an input slot antenna, a two-stage pHEMT amplifier cell in a microstrip form, and an output patch antenna. The signal is captured on the input side by the slot antenna fabricated on the ground plane of the microstrip. The position of the pickup loop with respect to the slot center was selected for easy matching into the amplifier cell. The signal got amplified by the two-stage amplifier cell and was delivered to the patch antenna for radiation into the output waveguide. The output patch antenna was orthogonally polarized to the incoming wave and was driven by a pair of amplifier cells in a push–pull configuration.

The cross section of the amplifier chip is shown in Fig. 5, illustrating the packaging details of the PWA. The GaAs chip containing the input/output antennas and the active amplifiers was mounted on an AlN chip carrier. The AlN chip carrier doubles in function to a provide heat-removal path for thermal management and also electrically loads the input slot antenna to have higher gain toward the signal source. The GaAs chip mounted on the AlN chip carrier was placed in the center section. Three metal pieces were finally assembled together for measurement using a standard waveguide setup.

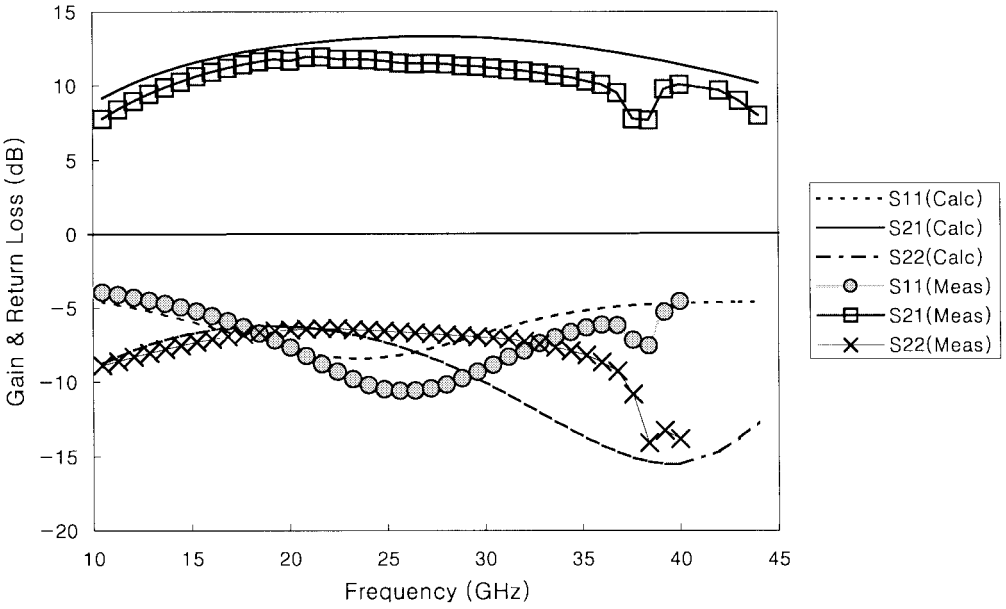

Fig. 6. Measured gain and return loss of the unit cell.

V. Measured Results of Unit Cell

A monolithic PWA was fabricated with a pHEMT MMIC process. The pHEMT's used in the circuit had 0.22-μm-long mushroom-shaped T-gates. To improve the threshold–voltage uniformity, gates were fabricated using a dry-recess process instead of the more conventional wet-etching process. Since all the unit cells share gate and drain bias, very good threshold voltage ($V_{\rm th}$) uniformity is required for the transistors to operate at the same current level. The dry-recess MMIC process improves threshold voltage uniformity, as shown in [10].

Test structures were simultaneously fabricated on the same wafer so that the unit cell can be tested by on-wafer probing. The unit cell was tested under a 50-Ω environment. Measured S-parameters of the unit cell are shown in Fig. 6. Vector measurements using on-wafer probing were performed up to 40 GHz. For additional measurements at 42, 43, and 44 GHz, the unit cell was mounted in a custom-made test fixture, and only S_{21} was measured by scalar measurements. The same test fixture was used for subsequent power measurements. The measured S_{21} shows ultrabroad-band characteristics, showing better than 8-dB gain from 12 to 44 GHz. At the design frequency of 44 GHz, the small-signal gain was 8 dB. Input and output matching was tested up to 40 GHz using a vector network analyzer. A lossy input-matching network resulted in a broad-band input match. Good output match was found near 40 GHz. Also shown in Fig. 6 are simulated S-parameters of the single-cell amplifier under 50-Ω termination for comparison. Measured and modeled S-parameters were in good agreement.

Power characteristics of the unit cell were also tested. The chip was mounted on the previously mentioned test fixture for this measurement. The output power and dc–RF efficiency versus input power is plotted in Fig. 7. The output power at $V_{\rm DD} = 8$ V was approximately 15 dBm (31 mW) and the corresponding drain efficiency was approximately 10%. As can be seen from Fig. 7, the output power is a strong function of

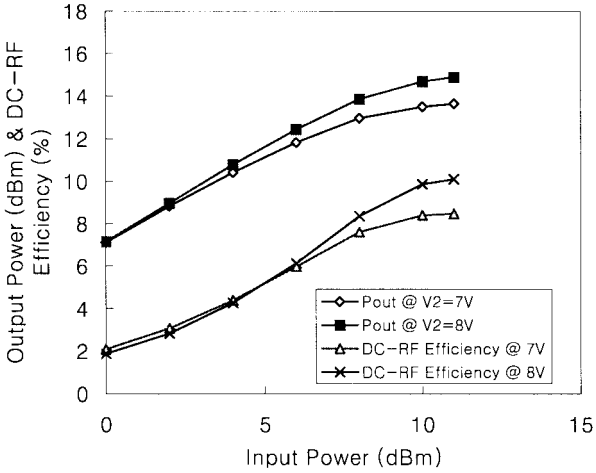

Fig. 7. Power characteristics of the unit cell for two different drain bias points.

$V_{\rm DD}$. Currently, maximum $V_{\rm DD}$ and output power is limited by the relatively low breakdown voltage of the pHEMT ($\sim$5 V).

VI. Measured Results of Waveguide PWA

The waveguide PWA consisting of 7×8 pHEMT amplifiers was tested in a WR-19 waveguide setup described in [4]. Measurement was performed in a fully closed waveguide. It was, therefore, possible to eliminate any diffraction losses, and measured results were true "flange-to-flange" results. The measured gain versus frequency is shown in Fig. 8. No corrections were made for the fixture losses. Unlike [4], the gain peaked exactly at the design frequency of 44 GHz, and was 5 dB. This was due to the modified design of the output patch antenna and improved feedback design of the unit cell. The amplifier had 3-dB bandwidth of 2.4 GHz or 5%. The array gain was still 3 dB lower than the small-signal gain of the unit cell. The 3-dB difference in the gain is attributed mostly to the poor radiation efficiency of the output patch antenna ($\sim$50%). The measured output power at $V_{\rm DD} = 8$ V was

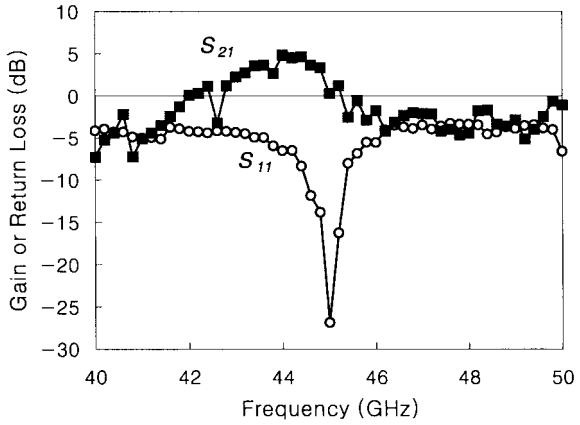

Fig. 8. Measured "flange-to-flange" gain and input return loss of the waveguide PWA.

approximately 300 mW, which was significantly lower than the expected output power estimated from the unit cell output power. Possible explanations are poor radiation efficiency of the patch antenna and nonuniform distribution of the power density inside the array. Currently, antenna design is being modified to increase the output power level. Another reason for lower output power in the array is the thermal problem. Unlike the single cells, which consume only 0.3 W, the whole array consumes more than 10 W, resulting in highly elevated temperatures in the center of the array. The output power of the single cells, especially those in the center of the array, is thus reduced. Degradation in the array output power by 2–3 dBm is attributed to this thermal problem. Better thermal management is under investigation for higher output power.

VII. Conclusions

An ultra-compact unit cell was designed for quasi-optic amplifier applications. The unit cell design was based on a directly coupled topology and was able to satisfy bias, stability, and size requirements of waveguide PWA's. The two-stage cell was realized in a chip size of 0.8 mm^2 and showed 8-dB small-signal gain with 15-dBm output power. The 7×8 amplifier array has been fabricated using this unit cell design. The amplifier array showed 5-dB small-signal gain at the design frequency of 44 GHz with 3-dB bandwidth of approximately 5%. An output power of 0.3 W was measured out of the waveguide flange.

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Emilio A. Sovero (M'85), photograph and biography not available at the time of publication.

Don S. Deakin, photograph and biography not available at the time of publication.

J. Aiden Higgins (M'62–SM'78), photograph and biography not available at the time of publication.